P20640B - a 32 Channel ASIC for Photon Energy and Timing Measurement

Keywords: Event building, Streaming readout, Photon detector readout, Multichannel ADC

Technical Summary

Pacific Microchip Corp. has developed P20640B ASIC - a power efficient 32-channel device for X- and gamma-ray energy and timing measurement and recording of pre- and post-event signal samples.

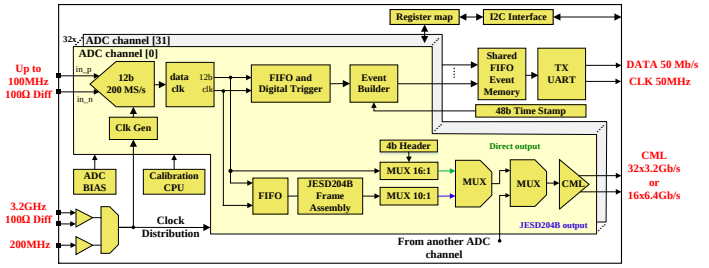


Figure 1. A block diagram of the ASIC.

Figure 2. A chip photo (left), BGA packaged ASIC (center) and the package ball array (right).

The ASIC supports applications in streaming readout of single photon sensitive detector instruments for event related energy and timing measurement. Timing, pulse duration, amplitude and other characteristics of each detected event in each channel is represented by a 124-bit packet and readout. The ASIC can also operate as a 32-channel ADC array with a JESD204B standard interface.

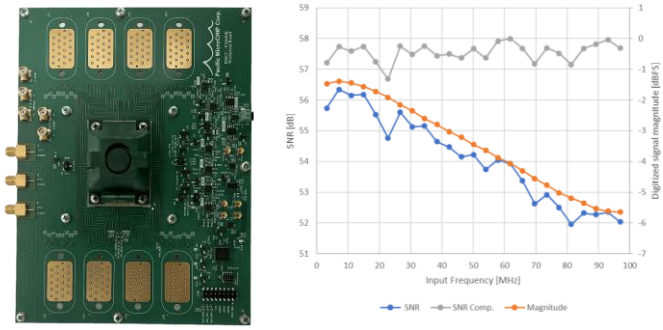


Figure 3. ASIC eval. PCB and measured ADC parameters.

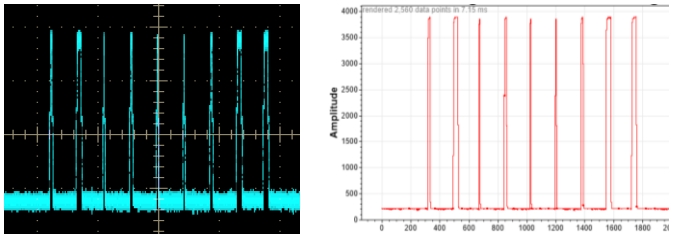


Figure 4. Pulses supplied to the ASIC channel (left). Pulses reconstructed from event builder data (right).

Targeted Operational Capabilities

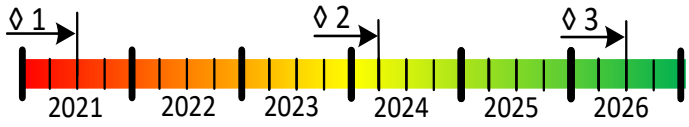
The ASIC offers low power consumption combined with complex functionality required for signal digitizing and extracting of event related data (time of arrival, threshold, time of peak, peak value, time over threshold, etc.). This data is assembled into packets and shipped out through an UART interface. Specific parameters/capabilities:

- 32 independently operated channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input swing
- Digitizing ENOB up to 10-bit
- Input signal bandwidth > 0.2GHz
- Pre- and post-event sample readout
- Integrated 32ch event-building digital back-end
- RISK CPU for ADC calibration
- Optional direct ADC output through JESD204B interface
- Event data packet output through UART interface
- Power consumption < 11.7mW/channel (JESD204B is off)
- Total power with ADC data interface <1.1W
- I2C interface for ASIC control
- Chip layout footprint 7.8mm^2
- 15mm x 15mm 324 (18x18) ball BGA package

Development Objectives & Milestones

The Phase I project demonstrated the feasibility of the ASIC. Withing the Phase II project the ASIC 1st prototype was designed, fabricated and tested. Within Phase IIB we produced the 2nd generation ASIC which is currently being testing. The project milestones include:

◊ 1. P20640A prototype chip is fabricated and tested (Ph. II)
◊ 2. Modified P20640B ASIC is produced, being sampled (Ph. IIB)
◊ 3. Final P20640C ASIC is fabricated, tested, sales started (Ph. IIC)



Applications

- NP/HEP Detector streaming readout
- Multichannel gamma-ray spectroscopy systems
- X-ray detectors
- CT systems, luggage, and cargo scanners
- Synthetic aperture spectrometer instruments
- Test and measurement instrumentation
- Multichannel data acquisition devices
- Synthetic aperture radars and lidars
- LIDARs

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